MAC9D, MAC9M, MAC9N

Preferred Device

Triacs

Silicon Bidirectional Thyristors

Designed for high performance full-wave ac control applications where high noise immunity and high commutating di/dt are required.

Features

- Blocking Voltage to 800 Volts
- On-State Current Rating of 8.0 Amperes RMS at 100°C
- Uniform Gate Trigger Currents in Three Quadrants
- High Immunity to dv/dt − 500 V/μs minimum at 125°C
- Minimizes Snubber Networks for Protection
- Industry Standard TO-220AB Package
- High Commutating di/dt − 6.5 A/ms minimum at 125°C
- Pb−Free Packages are Available*

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Peak Repetitive Off−State Voltage (Note 1) (T_J = −40 to 125°C, Sine Wave, 50 to 60 Hz, Gate Open) MAC9D MAC9M MAC9N	V_{DRM}, V_{RRM}	 400 600 800	V
On-State RMS Current (Full Cycle Sine Wave, 60 Hz, T_C = 100°C)	$I_{T(RMS)}$	8.0	A
Peak Non-Repetitive Surge Current (One Full Cycle Sine Wave, 60 Hz, T_J = 125°C)	I_{TSM}	80	A
Circuit Fusing Consideration (t = 8.3 ms)	I^2t	26	A^2sec
Peak Gate Power (Pulse Width ≤ 1.0 μs, T_C = 80°C)	P_{GM}	16	W
Average Gate Power (t = 8.3 ms, T_C = 80°C)	$P_{G(AV)}$	0.35	W
Operating Junction Temperature Range	T_J	−40 to +125	°C
Storage Temperature Range	T_{stg}	−40 to +150	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. V_{DRM} and V_{RRM} for all types can be applied on a continuous basis. Blocking voltages shall not be tested with a constant current source such that the voltage ratings of the devices are exceeded.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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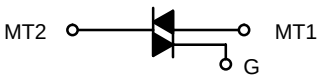
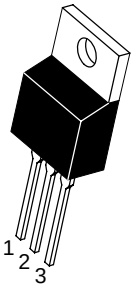
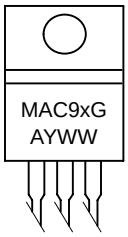
TRIACS
8 AMPERES RMS
400 thru 800 VOLTS



MARKING DIAGRAM



TO−220AB
CASE 221A−09
STYLE 4



x = D, M, or N
A = Assembly Location
Y = Year
WW = Work Week
G = Pb−Free Package

PIN ASSIGNMENT	
1	Main Terminal 1
2	Main Terminal 2
3	Gate
4	Main Terminal 2

ORDERING INFORMATION

Device	Package	Shipping
MAC9D	TO−220AB	50 Units / Rail
MAC9DG	TO−220AB (Pb−Free)	50 Units / Rail
MAC9M	TO−220AB	50 Units / Rail
MAC9MG	TO−220AB (Pb−Free)	50 Units / Rail
MAC9N	TO−220AB	50 Units / Rail
MAC9NG	TO−220AB (Pb−Free)	50 Units / Rail

Preferred devices are recommended choices for future use and best overall value.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction−to−Case Junction−to−Ambient	$R_{\theta JC}$ $R_{\theta JA}$	2.2 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes 1/8″ from Case for 10 Seconds	T_L	260	°C

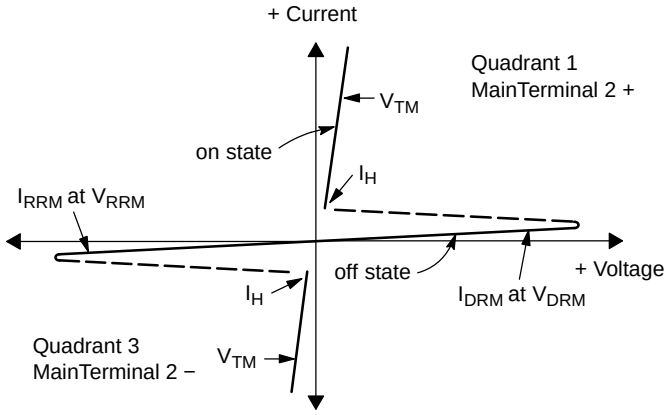
ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted; Electricals apply in both directions)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Peak Repetitive Blocking Current (V_D = Rated V_{DRM}, V_{RRM}; Gate Open) T_J = 25°C T_J = 125°C	I_{DRM}, I_{RRM}	 − −	 − −	 0.01 2.0	mA
ON CHARACTERISTICS					
Peak On-State Voltage (Note 2) (I_{TM} = ±11 A Peak)	V_{TM}	−	1.2	1.6	V
Gate Trigger Current (Continuous dc) (V_D = 12 V, R_L = 100 Ω) MT2(+), G(+) MT2(+), G(−) MT2(−), G(−)	I_{GT}	 10 10 10	 16 18 22	 50 50 50	mA
Holding Current (V_D = 12 V, Gate Open, Initiating Current = ±150 mA)	I_H	−	30	50	mA
Latching Current (V_D = 24 V, I_G = 50 mA) MT2(+), G(+); MT2(−), G(−) MT2(+), G(−)	I_L	 − −	 20 30	 50 80	mA
Gate Trigger Voltage (V_D = 12 V, R_L = 100 Ω) MT2(+), G(+) MT2(+), G(−) MT2(−), G(−)	V_{GT}	 0.5 0.5 0.5	 0.69 0.77 0.72	 1.5 1.5 1.5	V
Gate Non−Trigger Voltage (V_D = 12 V, R_L = 100 Ω, T_J = 125°C) MT2(+), G(+); MT2(+), G(−); MT2(−), G(−)	V_{GD}	 0.2	 −	 −	V
DYNAMIC CHARACTERISTICS					
Rate of Change of Commutating Current; See Figure 10. (V_D = 400 V, I_{TM} = 4.4 A, Commutating dv/dt = 18 V/μs, Gate Open, T_J = 125°C, f = 250 Hz, No Snubber) C_L = 10 μF L_L = 40 mH	$(di/dt)_c$	6.5	−		A/ms
Critical Rate of Rise of Off-State Voltage (V_D = Rated V_{DRM}, Exponential Waveform, Gate Open, T_J = 125°C)	dv/dt	500	−	−	V/μs

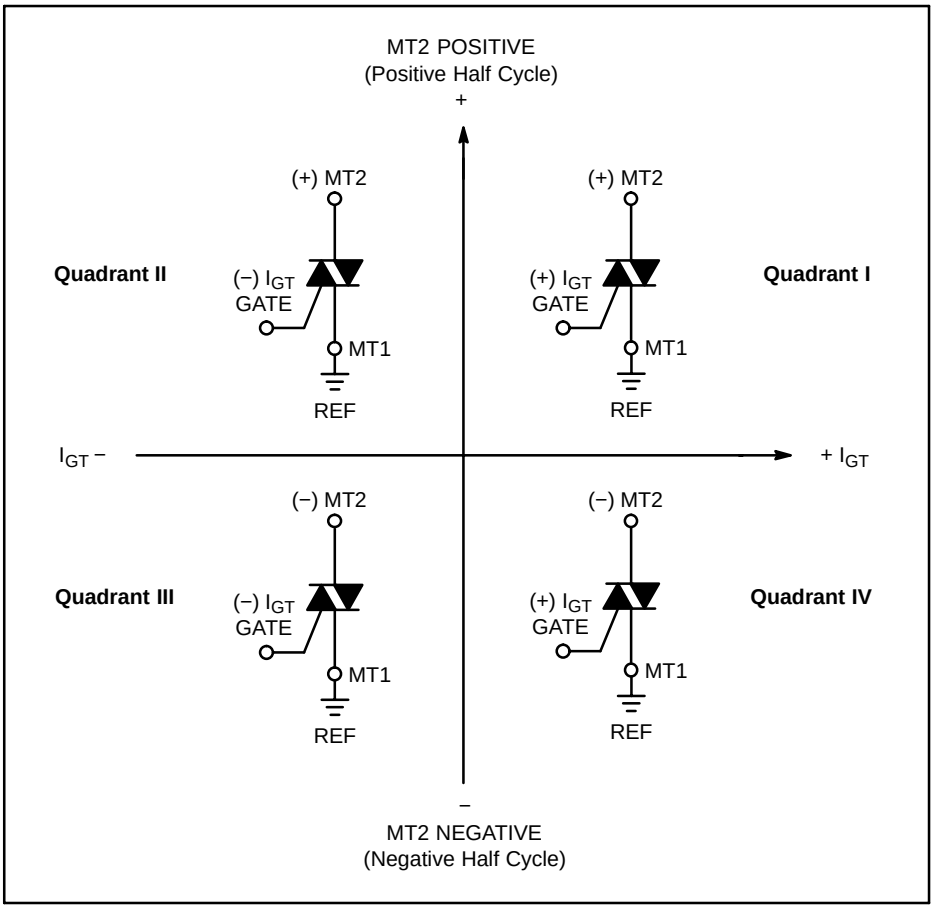
2. Indicates Pulse Test: Pulse Width ≤ 2.0 ms, Duty Cycle ≤ 2%.

Voltage Current Characteristic of Triacs (Bidirectional Device)

Symbol	Parameter
V_{DRM}	Peak Repetitive Forward Off State Voltage
I_{DRM}	Peak Forward Blocking Current
V_{RRM}	Peak Repetitive Reverse Off State Voltage
I_{RRM}	Peak Reverse Blocking Current
V_{TM}	Maximum On State Voltage
I_H	Holding Current



Quadrant Definitions for a Triac



All polarities are referenced to MT1.
With in−phase signals (using standard AC lines) quadrants I and III are used.

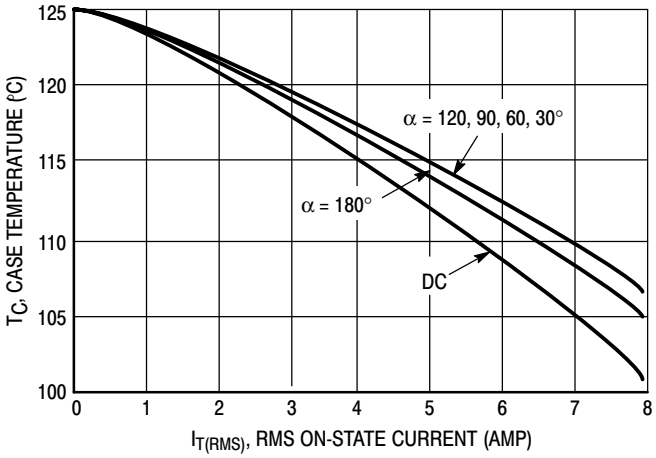


Figure 1. RMS Current Derating

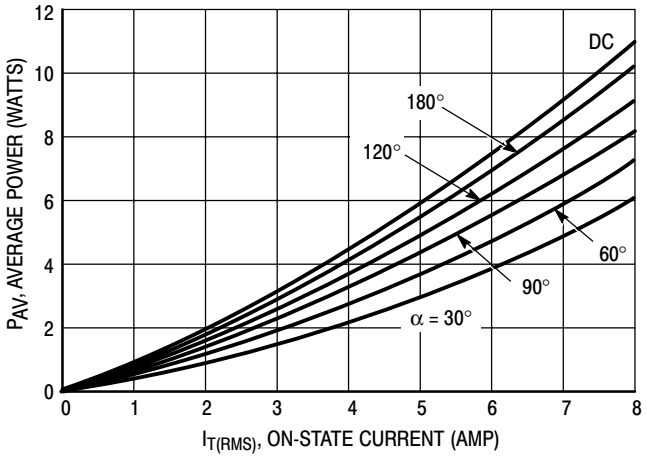


Figure 2. On-State Power Dissipation

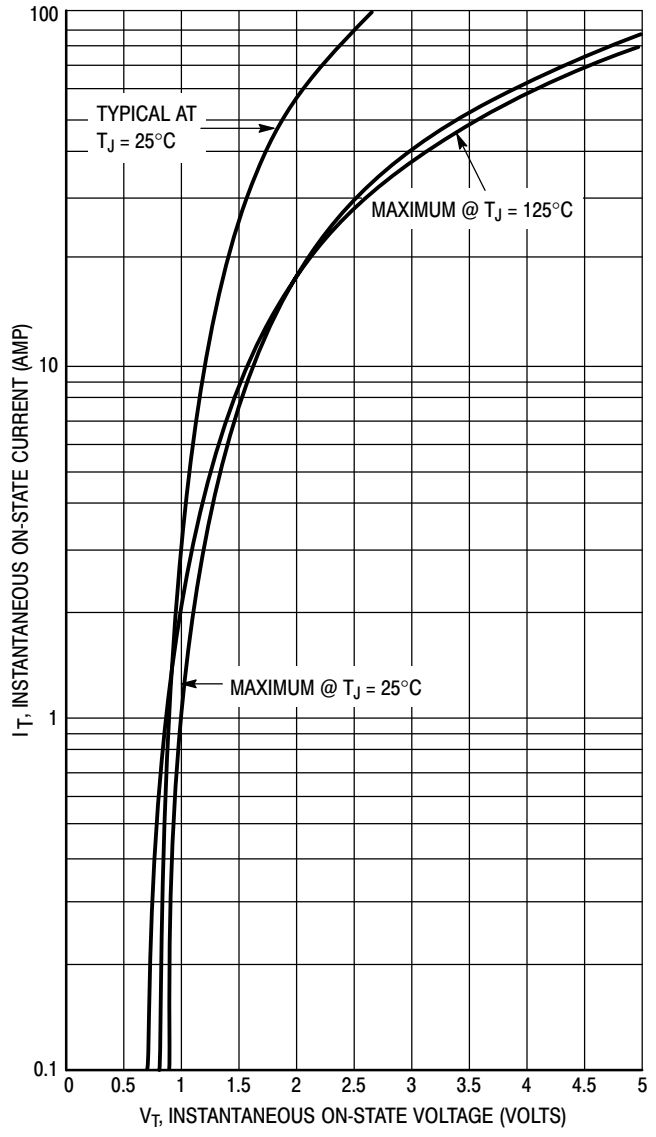


Figure 3. On-State Characteristics

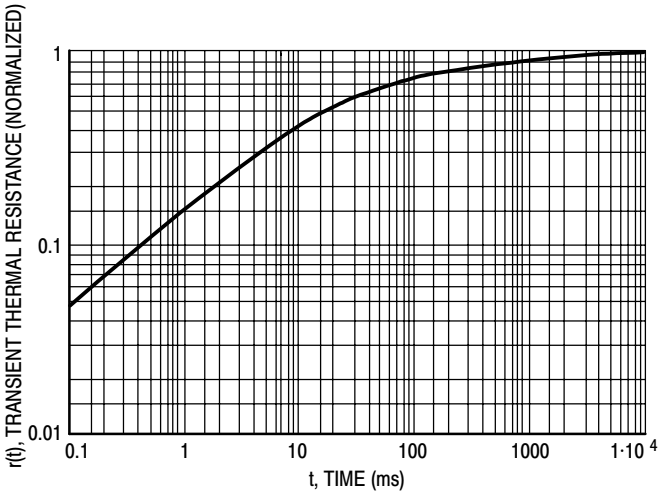


Figure 4. Thermal Response

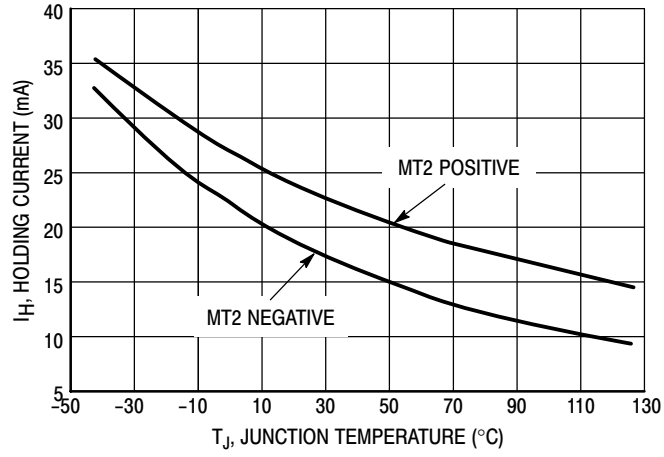


Figure 5. Holding Current Variation

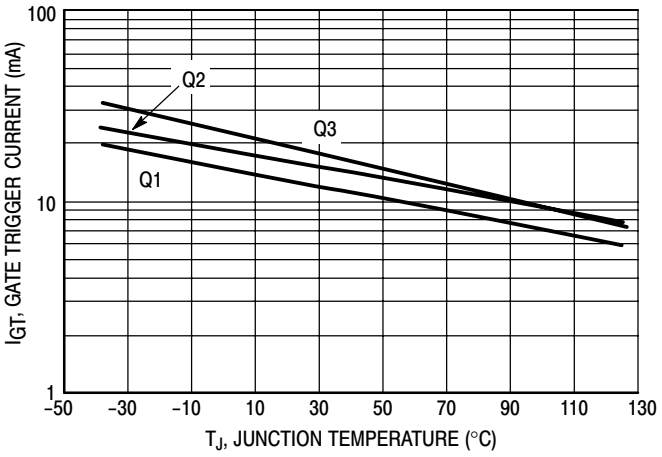


Figure 6. Gate Trigger Current Variation

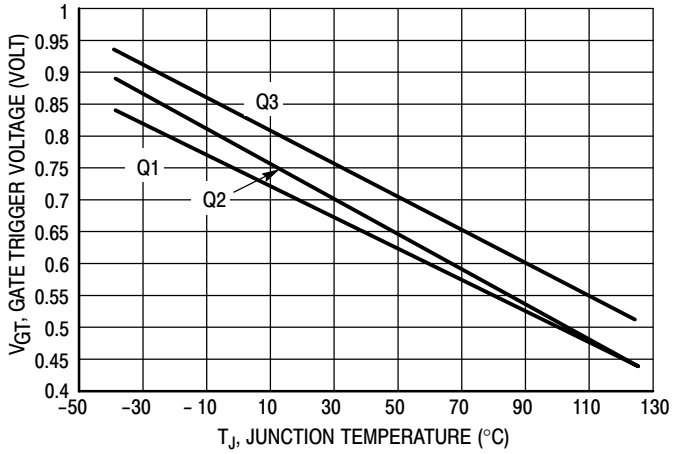


Figure 7. Gate Trigger Voltage Variation

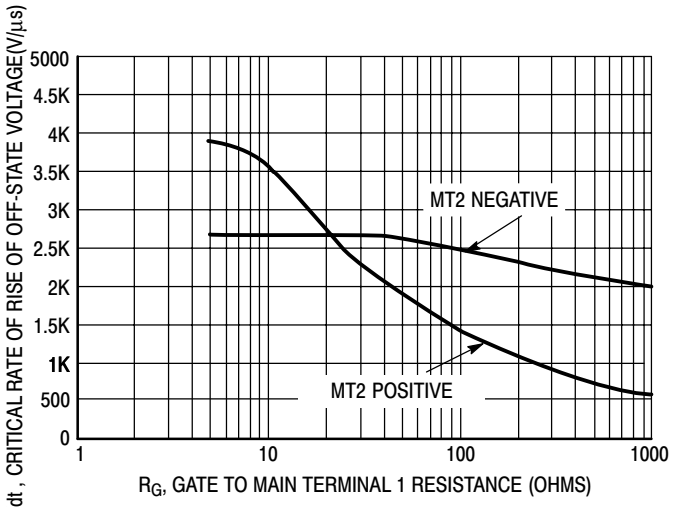


Figure 8. Critical Rate of Rise of Off-State Voltage (Exponential)

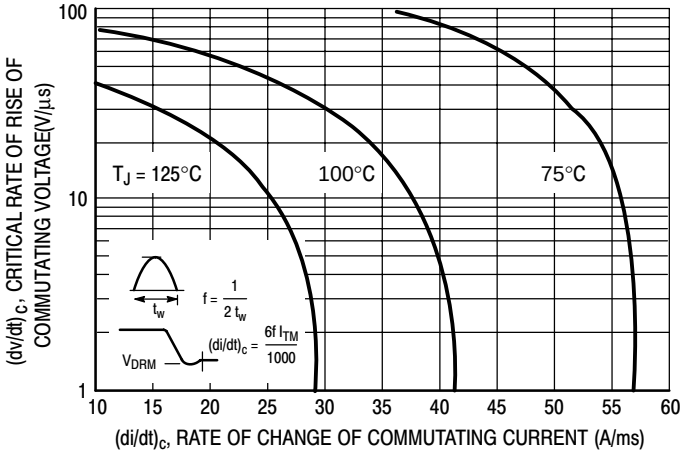
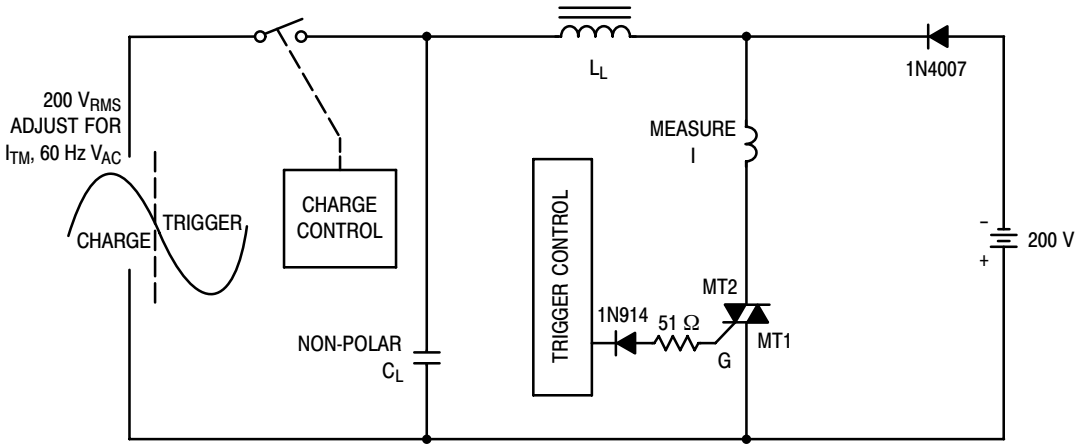


Figure 9. Critical Rate of Rise of Commutating Voltage

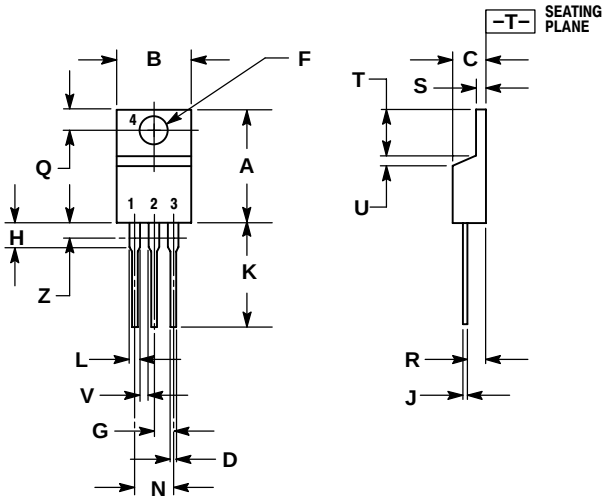


Note: Component values are for verification of rated $(di/dt)_c$. See AN1048 for additional information.

Figure 10. Simplified Test Circuit to Measure the Critical Rate of Rise of Commutating Current $(di/dt)_c$

PACKAGE DIMENSIONS

TO−220AB
CASE 221A−09
ISSUE AA



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

STYLE 4:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE
4. MAIN TERMINAL 2

PUBLICATION ORDERING INFORMATION

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